Claims

1. A semiconductor integrated circuit device comprising:

a plurality of internal circuits arranged internally in a circuit forming region, said internal circuits having difference power lines;

an inter-circuit signal wire arranged to interconnect said internal circuits; and

a plurality of active elements in another connection configuration including elements of an identical or similar structure to an active element in a first connection configuration connected to said inter-circuit signal wire, said active elements being arranged near said active element in the first connection configuration to sandwich or surround said active element in the first connection configuration, said active elements being connected to power lines of said internal circuits associated therewith and being isolated from signal wires other than said inter-circuit signal wire.

2. A semiconductor integrated circuit device according to claim 1, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition, and said active element in the first connection configuration and said active elements in the other connection configuration are allocated to some of said basic cells.

3. A semiconductor integrated circuit device according to

claim 1, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

4. A semiconductor integrated circuit device according to claim 3, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

5. A semiconductor integrated circuit device comprising:

a plurality of internal circuits arranged internally in a circuit forming region, said internal circuits having difference power lines;

an inter-circuit signal wire arranged to interconnect said internal circuits; and

an active element in a second connection configuration arranged near an active element in a first connection configuration connected to said inter-circuit signal wire, including an element of an identical or similar structure to said active element in the first connection configuration, said active element being connected to power lines of said internal circuits associated therewith and being isolated from said inter-circuit signal wire and other signal wires.

6. A semiconductor integrated circuit device according to claim 5, wherein a plurality of said active elements in the second connection configuration are arranged to sandwich or surround said

active element in the first connection configuration.

7. A semiconductor integrated circuit device according to claim 5, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition, and said active element in the first connection configuration and said active elements in the second connection configuration are allocated to some of said basic cells.

8. A semiconductor integrated circuit device according to claim 5, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

9. A semiconductor integrated circuit device according to claim 6, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

10. A semiconductor integrated circuit device according to claim 5, further comprising an active element in a third connection configuration, arranged near said active element in the first connection configuration and including an element of an identical or similar structure to said active element in the first connection configuration, said active element in the third connection configuration being connected to power lines of an internal circuit

associated therewith and said inter-circuit signal wire and being isolated from other signal lines.

11. A semiconductor integrated circuit device according to claim 10, wherein a plurality of said active elements in the third connection configuration are arranged to sandwich or surround said active element in the first connection configuration.

12. A semiconductor integrated circuit device according to claim 10, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition, and said active element in the first connection configuration, said active elements in the second connection configuration, and said active elements in the third connection configuration are allocated to some of said basic cells.

13. A semiconductor integrated circuit device according to claim 10, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

14. A semiconductor integrated circuit device according to claim 13, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

15. A semiconductor integrated circuit device according to claim 10, wherein:

a plurality of said inter-circuit signal wires having different communication directions from each other are arranged in any pair of said plurality of internal circuits;

said active element in the second connection configuration and said active element in the third connection configuration are arranged near said active element in the first connection configuration on a reception side of said inter-circuit signal wire in one of said pair of internal circuits; and

said active elements in the third connection configuration are arranged instead of or exclusive of said active element in the second connection configuration, near said active element in the first connection configuration on a reception side of said inter-circuit signal wire in the other of said pair of internal circuits.

16. A semiconductor integrated circuit device according to claim 15, wherein a group of elements including a plurality of either said active elements in the first connection configuration, said active elements in the second connection configuration, or said active elements in the third connection configuration are arranged to sandwich or surround said active element in the first connection configuration.

17. A semiconductor integrated circuit device according to

claim 15, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition, and said active element in the first connection configuration, said active elements in the second connection configuration, and said active elements in the third connection configuration are allocated to some of said basic cells.

18. A semiconductor integrated circuit device according to claim 15, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

19. A semiconductor integrated circuit device according to claim 18, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

20. A semiconductor integrated circuit device comprising:

a plurality of internal circuits arranged internally in a circuit forming region, said internal circuits having difference power lines;

an inter-circuit signal wire arranged to interconnect said internal circuits; and

an inter-circuit auxiliary wire connected to a static area near a location at which said inter-circuit signal wire is connected.

21. A semiconductor integrated circuit device according to claim 20, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition.

22. A semiconductor integrated circuit device according to claim 20, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

23. A semiconductor integrated circuit device according to claim 22, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

24. A semiconductor integrated circuit device according to claim 20, wherein said static area includes a partial region of an active element on a transmission side of said active elements in the first connection configuration connected to said inter-circuit signal wire, said partial region being connected to a power line of said internal circuit associated therewith, and an active element in another connection configuration having an identical or similar structure to said active element in the first connection configuration on a reception side, and arranged near said active element in the first connection configuration, said active element in the other connection configuration being isolated from signal

wires other than said inter-circuit auxiliary wire.

25. A semiconductor integrated circuit device according to claim 24, wherein a plurality of said active elements in the other connection configuration are arranged to sandwich or surround said active element in the first connection configuration.

26. A semiconductor integrated circuit device according to claim 24, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition, and said active element in the first connection configuration and said active elements in the other connection configuration are allocated to some of said basic cells.

27. A semiconductor integrated circuit device according to claim 24, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

28. A semiconductor integrated circuit device according to claim 27, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

29. A semiconductor integrated circuit device according to claim 24, wherein said inter-circuit auxiliary wire is connected to

a neighboring region overlapping with or close to said partial region on said power line connected thereto, instead of said partial region.

30. A semiconductor integrated circuit device according to claim 24, wherein:

a plurality of said inter-circuit signal wires having different communication directions from each other are arranged in any pair of said plurality of internal circuits;

an active element in a further connection configuration having an identical or similar structure to said active element in the other connection configuration is arranged in addition to said active element in the other connection configuration near an active element in the first connection configuration on a reception side of said inter-circuit signal wire in one of said pair of internal circuits, said active element in the further connection configuration being connected to a power line of said internal circuit and being isolated from said inter-circuit signal wire, other signal wires and said inter-circuit auxiliary wire; and

said active elements in the other connection configuration are arranged instead of or exclusive of said active element in the further connection configuration, near said active element in the first connection configuration on a reception side of said inter-circuit signal wire in the other of said pair of internal circuits.

31. A semiconductor integrated circuit device according to

claim 30, wherein a group of elements including a plurality of either said active elements in the first connection configuration, said active elements in the other connection configuration, or said active elements in the further connection configuration are arranged to sandwich or surround said active element in the first connection configuration.

32. A semiconductor integrated circuit device according to claim 30, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition, and said active element in the first connection configuration, said active elements in the other connection configuration, and said active elements in the further connection configuration are allocated to some of said basic cells.

33. A semiconductor integrated circuit device according to claim 30, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

34. A semiconductor integrated circuit device according to claim 33, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

35. A semiconductor integrated circuit device according to

claim 29, wherein:

a plurality of said inter-circuit signal wires having different communication directions from each other are arranged in any pair of said plurality of internal circuits;

an active element in a further connection configuration having an identical or similar structure to said active element in the other connection configuration is arranged in addition to said active element in the other connection configuration near an active element in the first connection configuration on a reception side of said inter-circuit signal wire in one of said pair of internal circuits, said active element in the further connection configuration being connected to a power line of said internal circuit and being isolated from said inter-circuit signal wire, other signal wires and said inter-circuit auxiliary wire; and

said active elements in the other connection configuration are arranged instead of or exclusive of said active element in the further connection configuration, near said active element in the first connection configuration on a reception side of said inter-circuit signal wire in the other of said pair of internal circuits.

36. A semiconductor integrated circuit device according to claim 35, wherein a group of elements including a plurality of either said active elements in the first connection configuration, said active elements in the other connection configuration, or said active elements in the further connection configuration are arranged to

sandwich or surround said active element in the first connection configuration.

37. A semiconductor integrated circuit device according to claim 35, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition, and said active element in the first connection configuration, said active elements in the other connection configuration, and said active elements in the further connection configuration are allocated to some of said basic cells.

38. A semiconductor integrated circuit device according to claim 35, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

39. A semiconductor integrated circuit device according to claim 38, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

40. A semiconductor integrated circuit device comprising:

a plurality of internal circuits arranged internally in a circuit forming region, said internal circuits having difference power lines;

a plurality of input/output circuits arranged outside said

internal circuits;

a plurality of external connection terminals outside said input/output circuits;

a signal wire passing through an input/output circuit in one of a plurality of sets comprised of any of said internal circuits and any of said input/output circuit, said plurality of sets being connected to common power lines, said signal wire reaching said internal circuit included in the same set as said input/output circuit from any of said external connection terminals;

a branched wire branched from said signal wire and passing through said input/output circuit in any other set of said plurality of sets, and reaching said internal circuit in the same set as said input/output circuit;

a first protection circuit arranged in said input/output circuit of said one set for said signal wire;

a second protection circuit arranged in said input/output circuit in another set for said branched wire; and

a third protection circuit arranged in said internal circuit in said other set for said branched wire.

41. A semiconductor integrated circuit device according to claim 40, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition.

42. A semiconductor integrated circuit device according to

claim 40, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

43. A semiconductor integrated circuit device according to claim 40, wherein said third protection circuit includes a plurality of protection elements, said protection elements being arranged to sandwich or surround an element to be protected.

44. A semiconductor integrated circuit device according to claim 40, wherein either of said first, second or third protection circuit includes an active element connected to a power line of an associated input/output circuit or an associated internal circuit, and isolated from any signal wire.

45. A semiconductor integrated circuit device according to claim 44, wherein said third protection circuit includes a plurality of protection elements, said protection elements being arranged to sandwich or surround an element to be protected.